

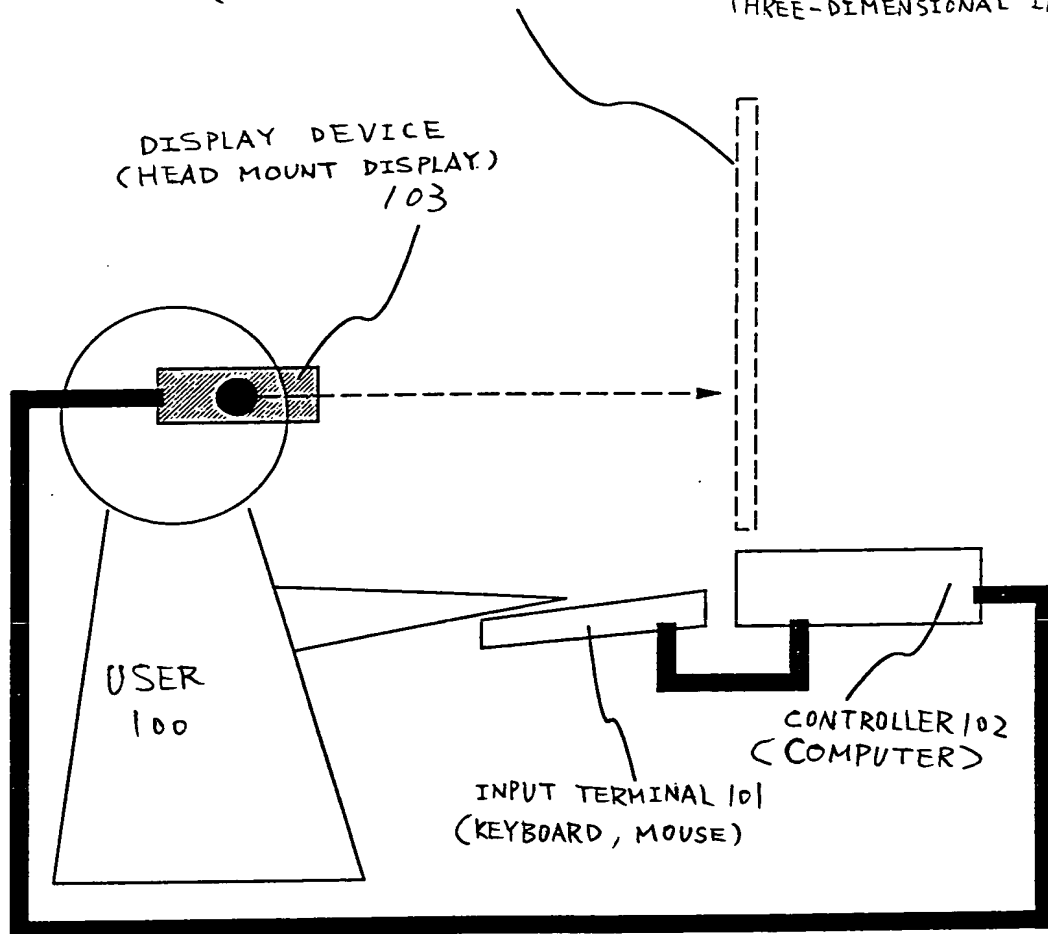
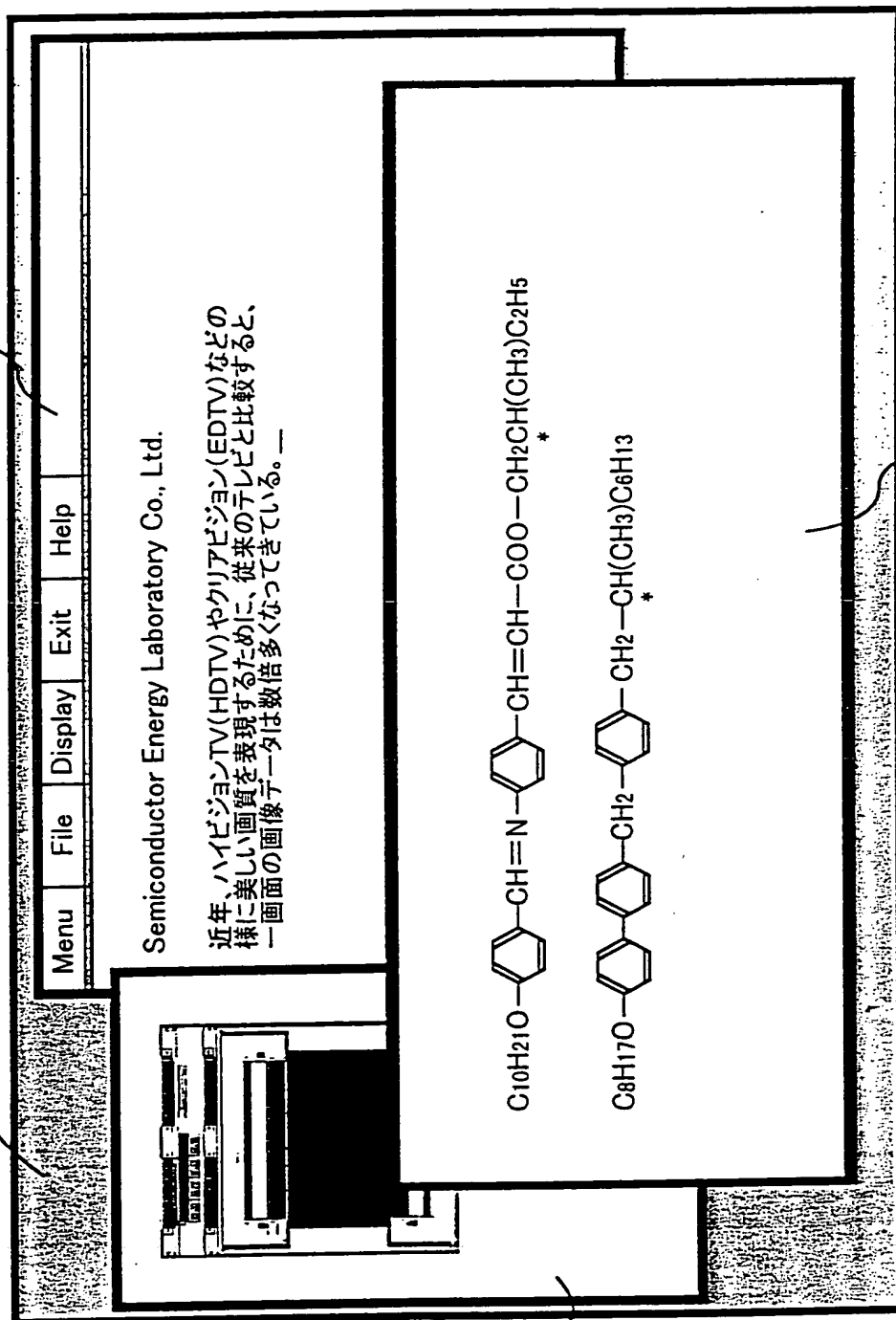
[illegible]

Fig. 1

Fig. 2

VIRTUAL DISPLAY SCREEN 104 WINDOW 203



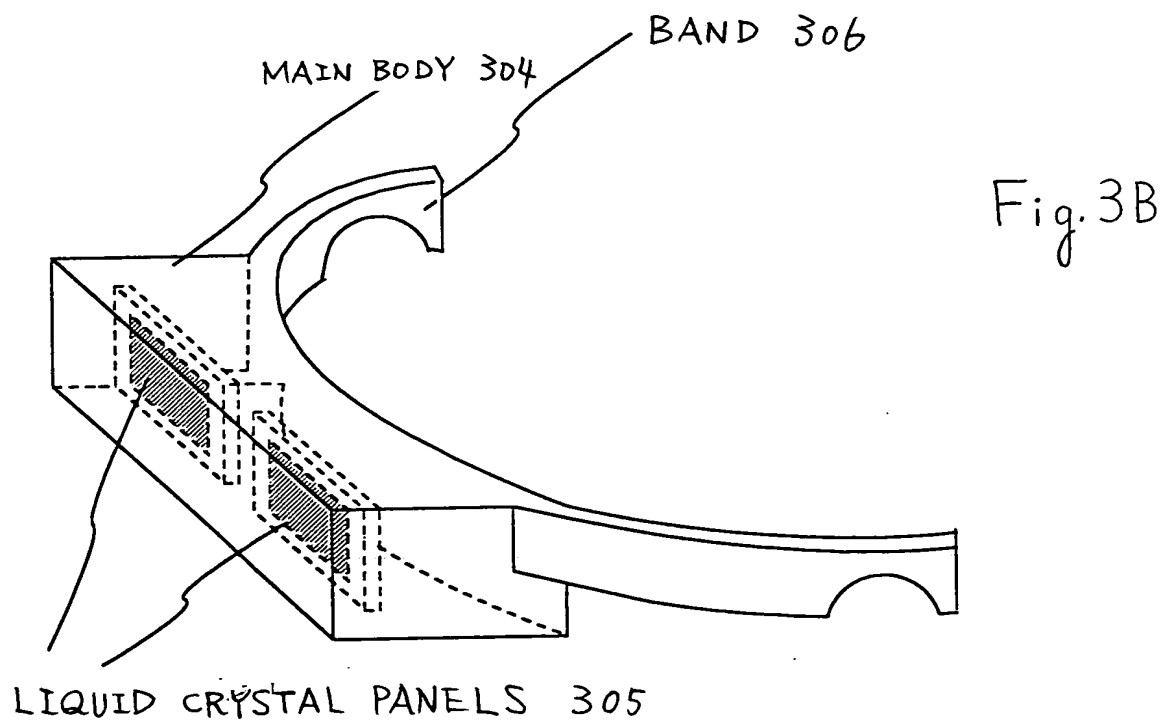
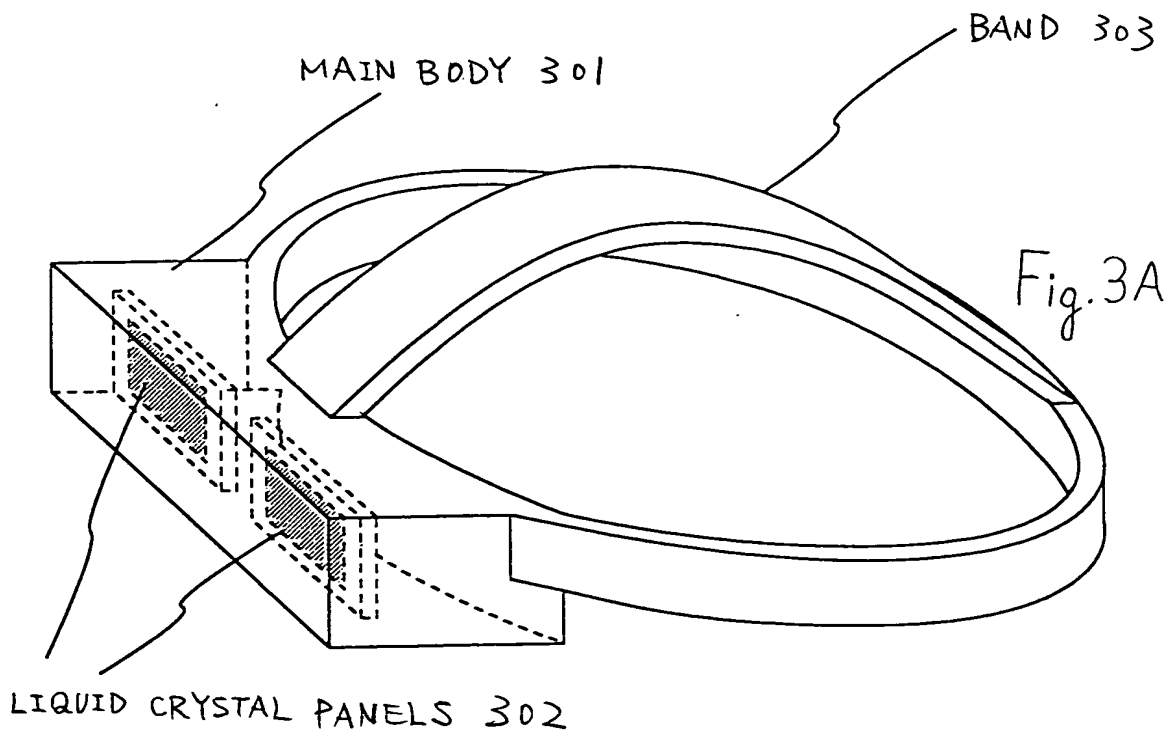
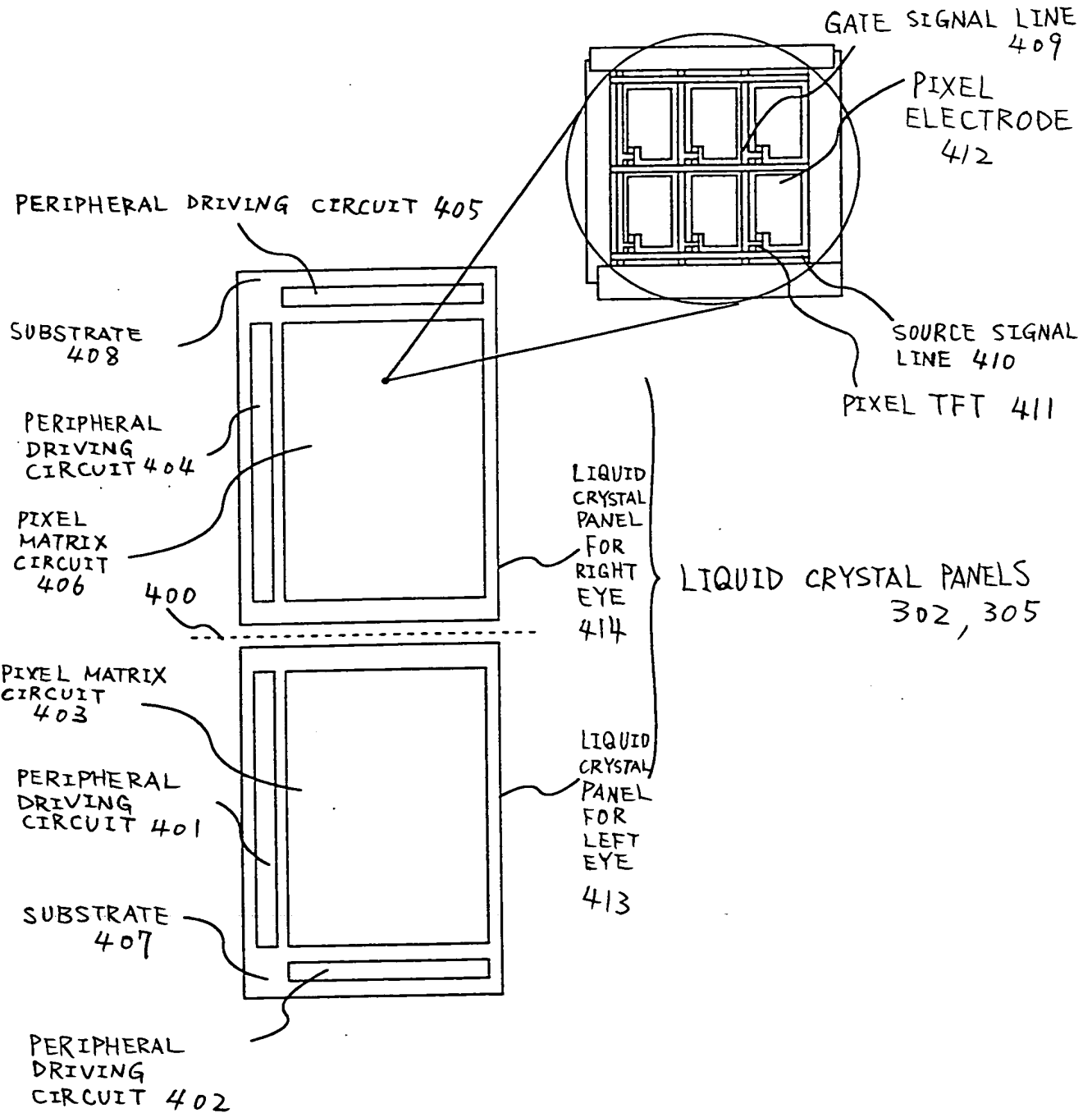
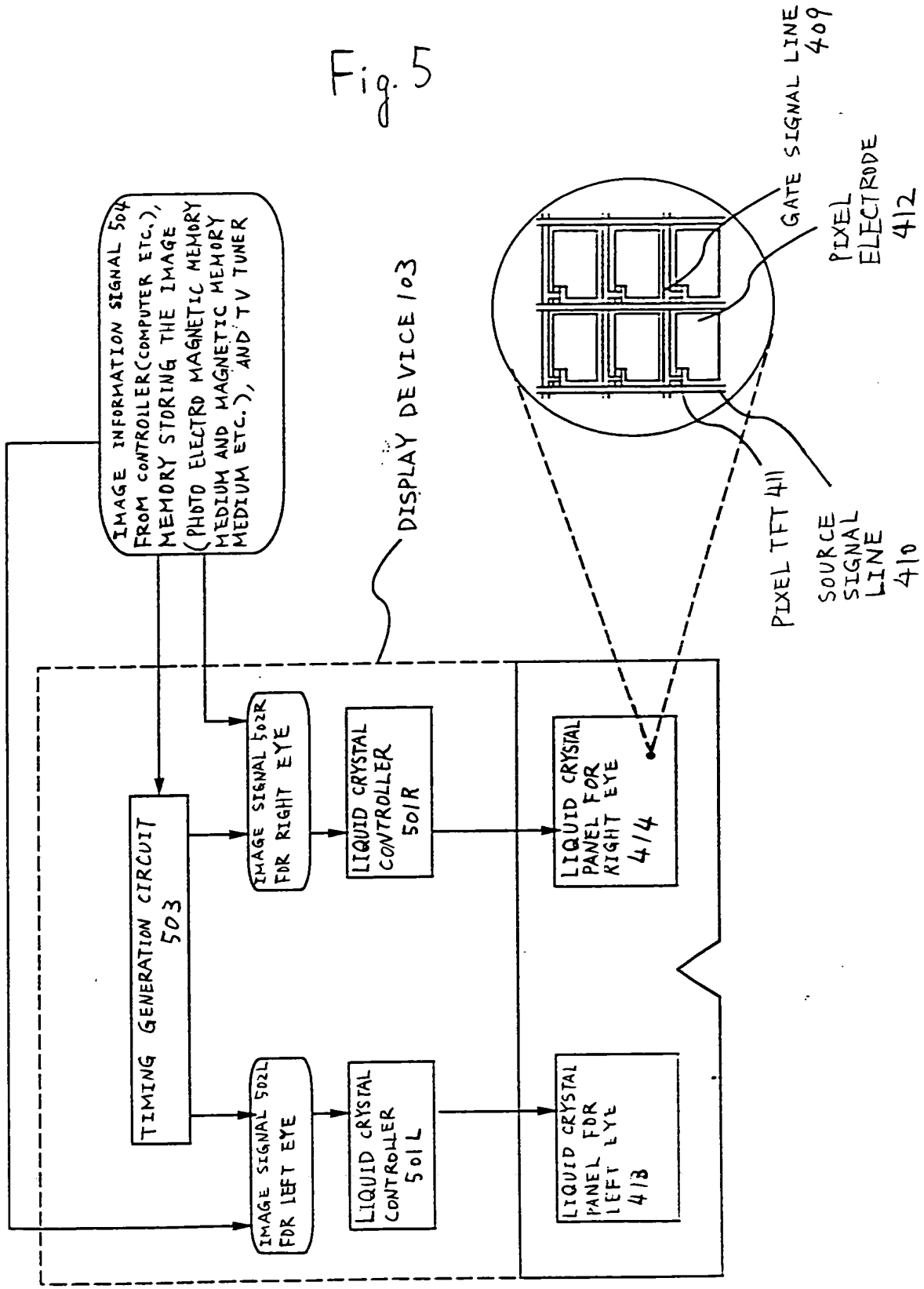


Fig. 4





VIRTUAL DISPLAY SCREEN 607
(DISPLAY SCREEN FOR TWO-DIMENSIONAL OR
THREE-DIMENSIONAL IMAGES)

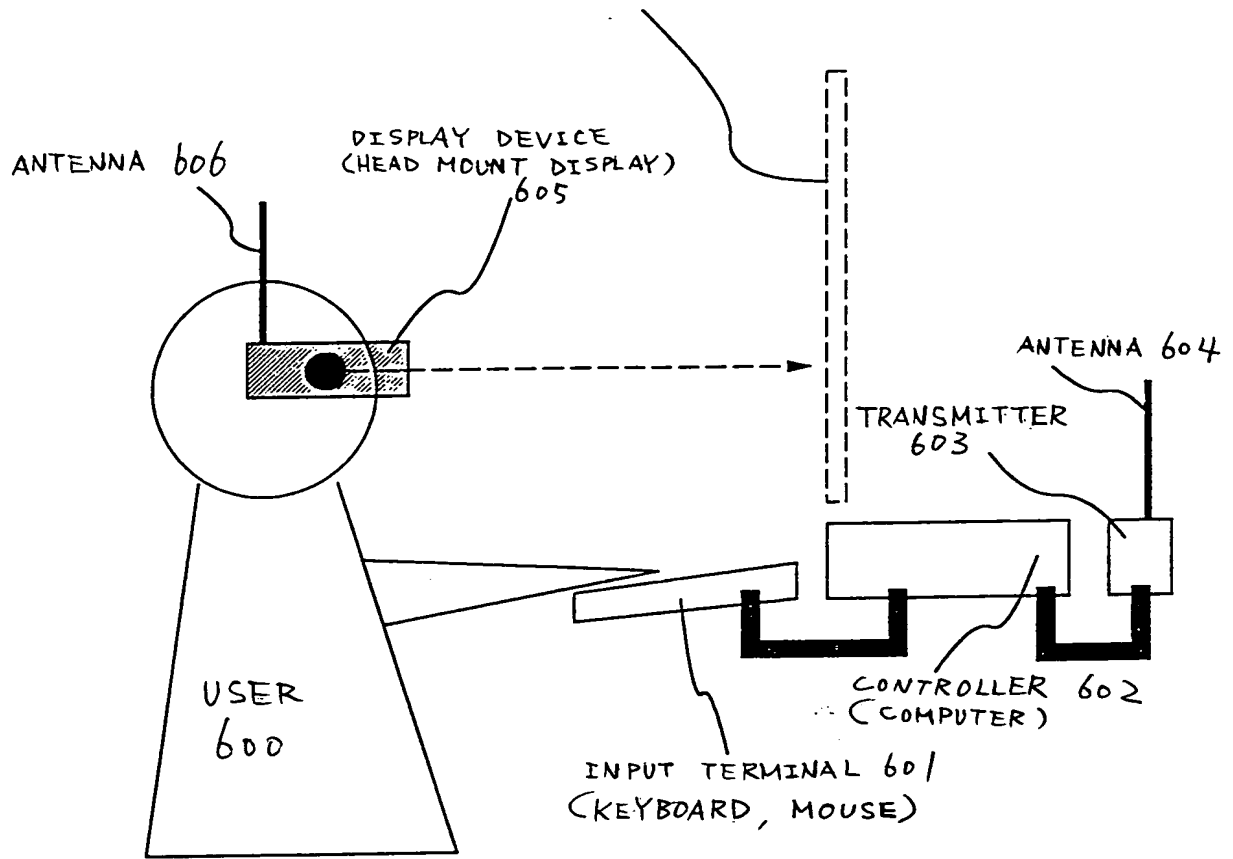


Fig. 6

00000-00000-00000

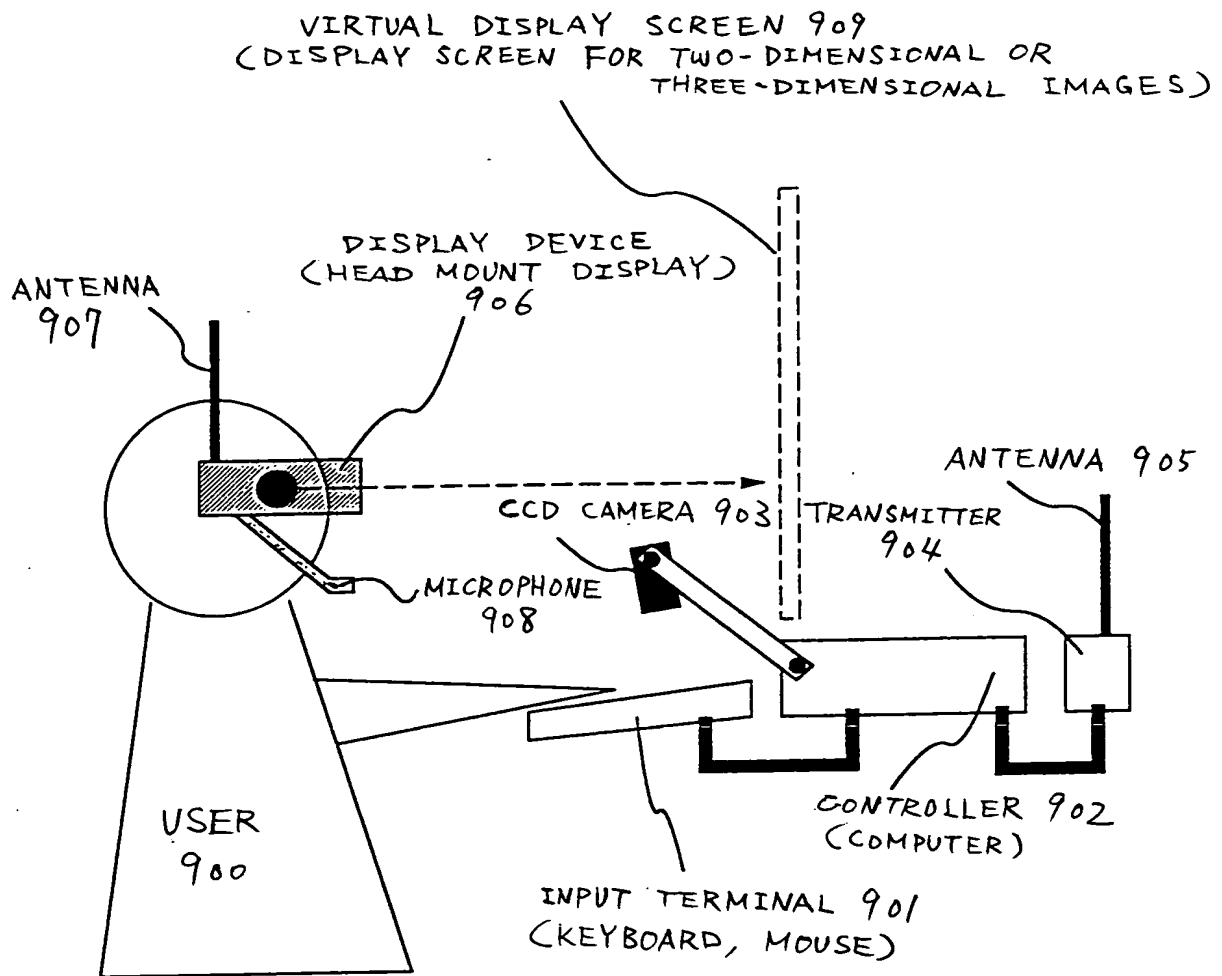


Fig. 9

VIRTUAL DISPLAY SCREEN 1010
 (DISPLAY SCREEN FOR TWO-DIMENSIONAL OR
 THREE-DIMENSIONAL IMAGES)

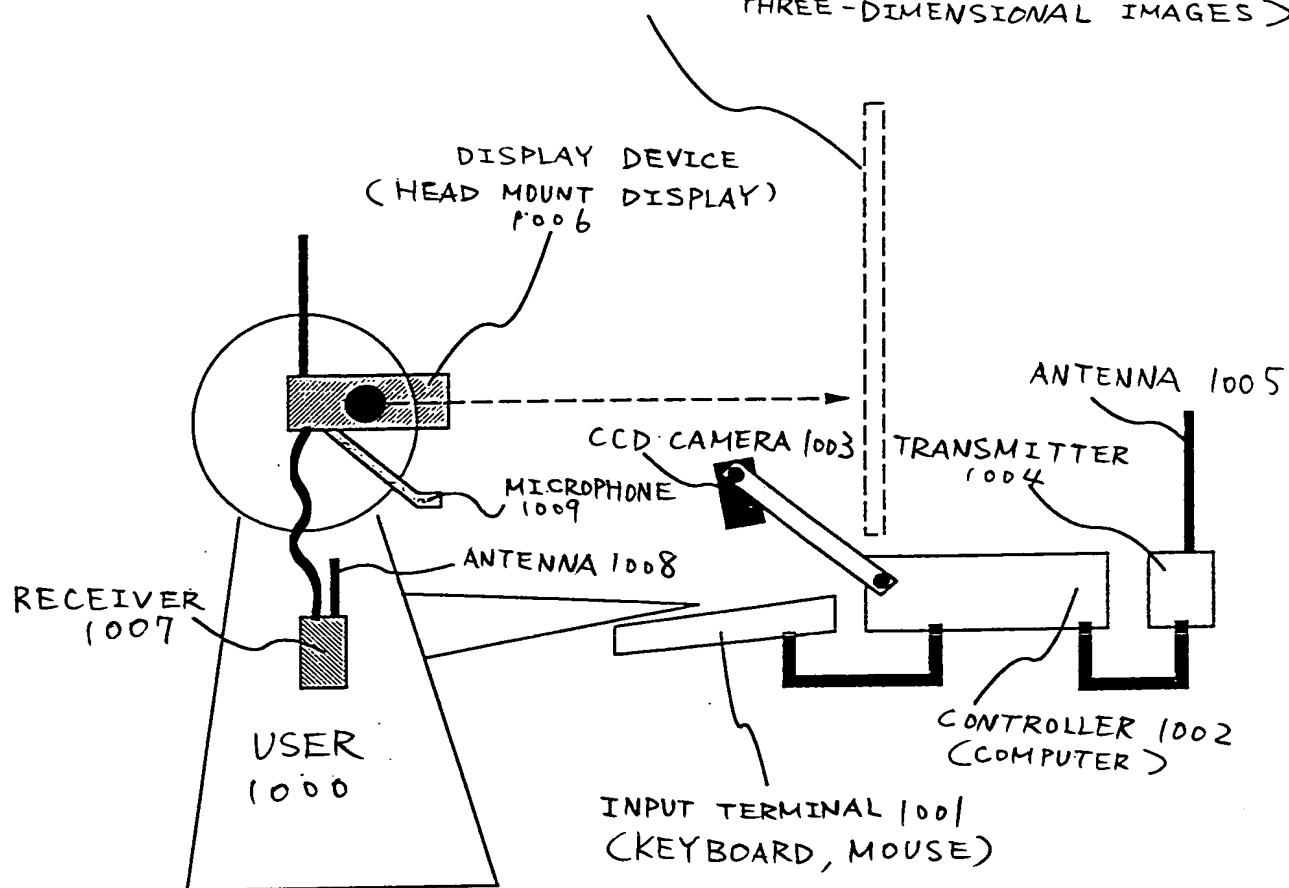


Fig. 10

VIRTUAL DISPLAY SCREEN 1104
(DISPLAY SCREEN FOR TWO-DIMENSIONAL OR
THREE-DIMENSIONAL IMAGES)

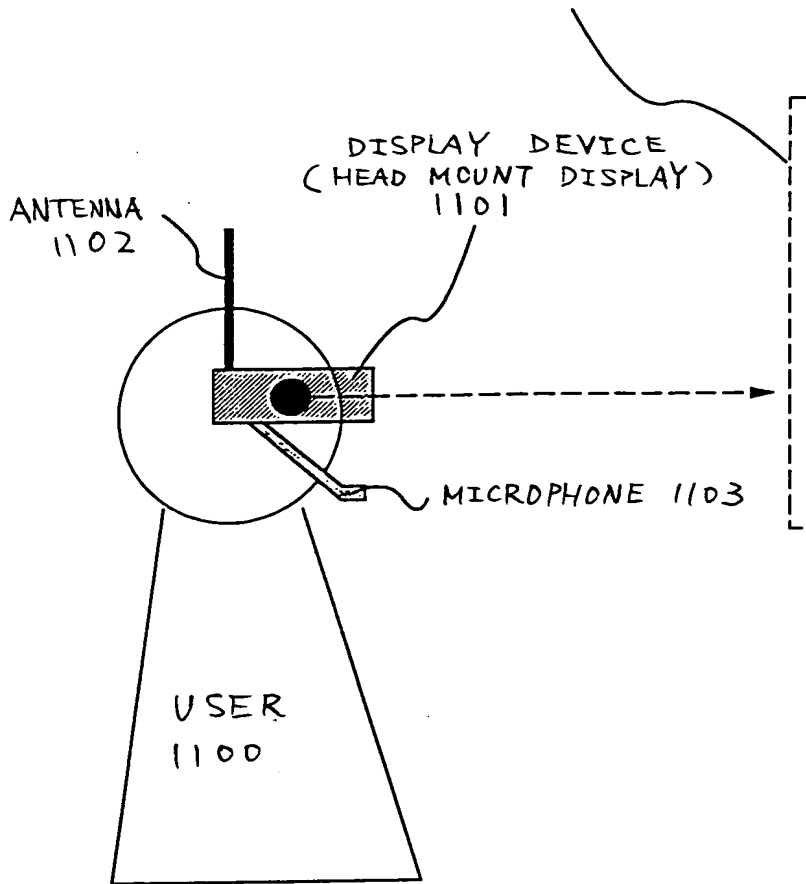


Fig. 11

000000-000000

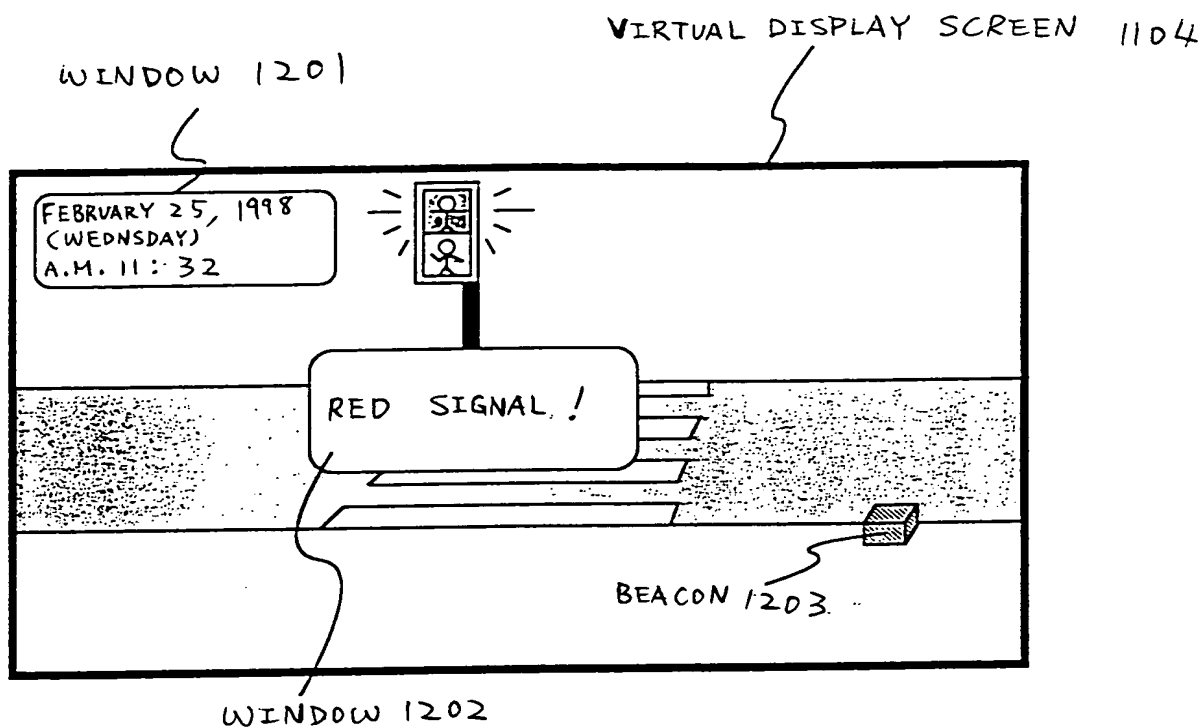


Fig. 12

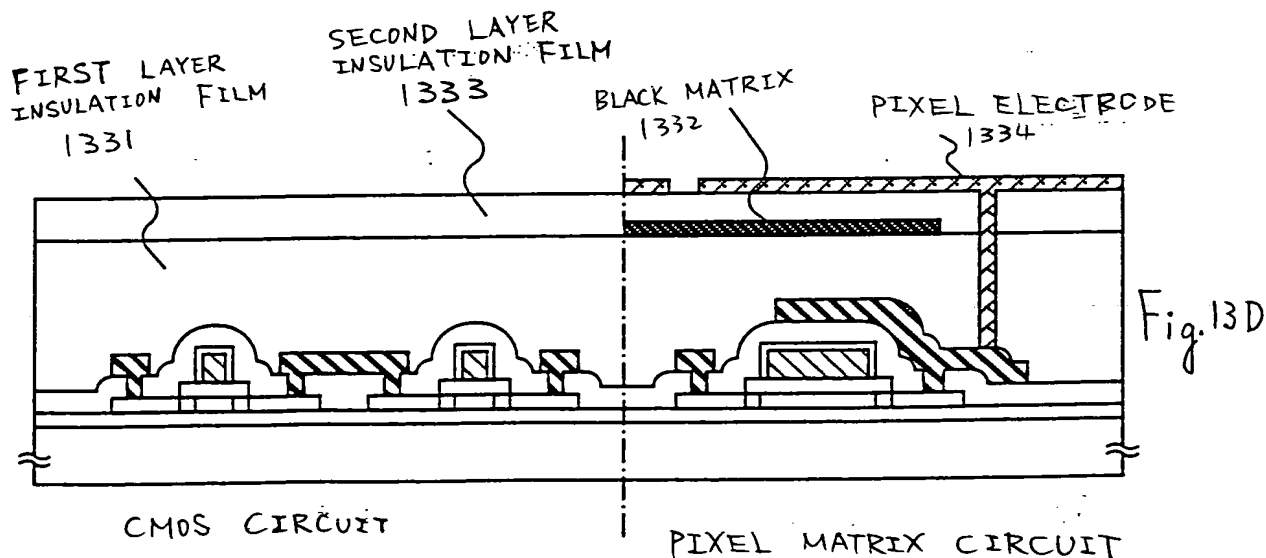
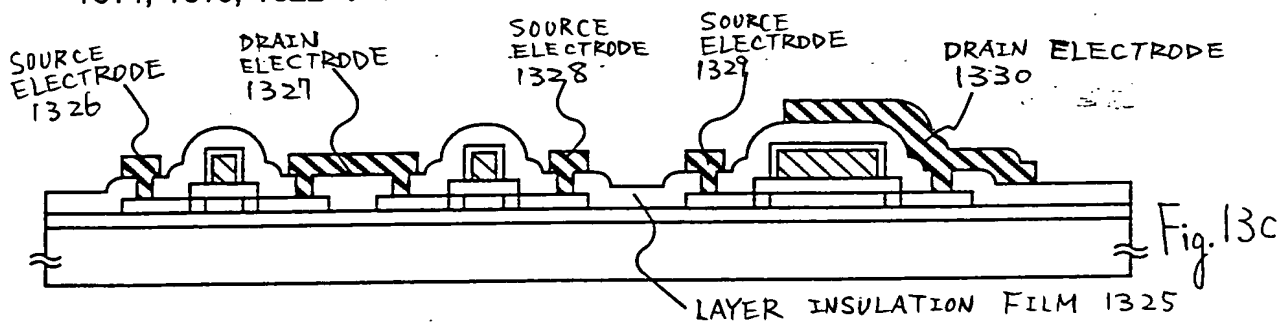
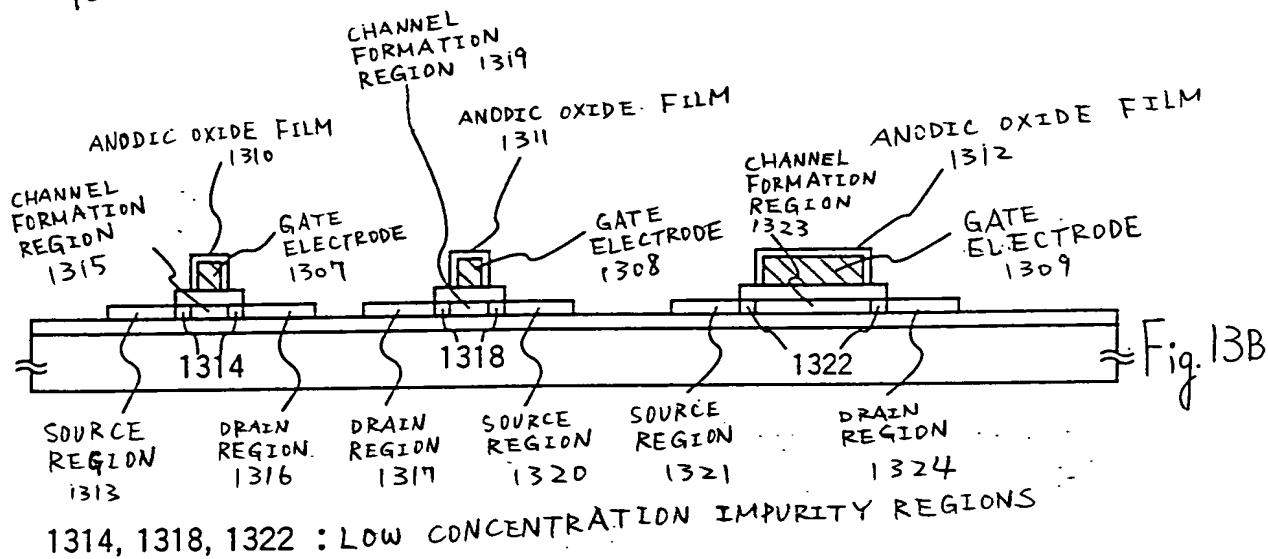
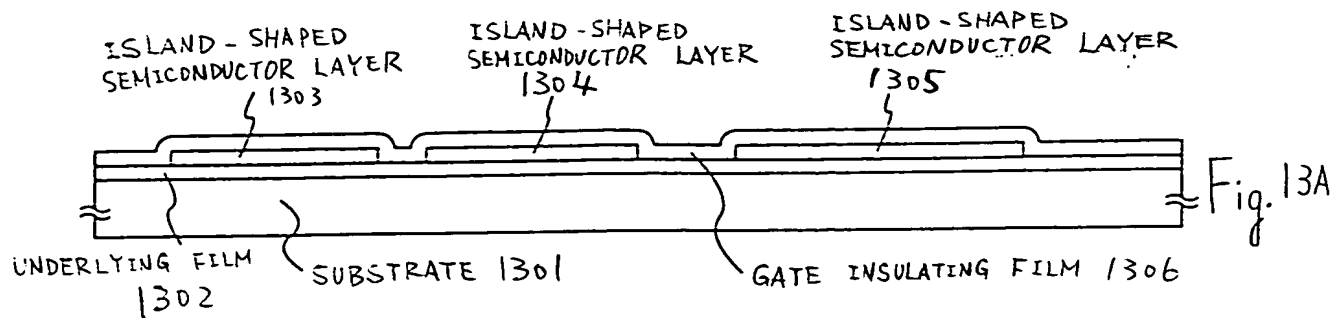
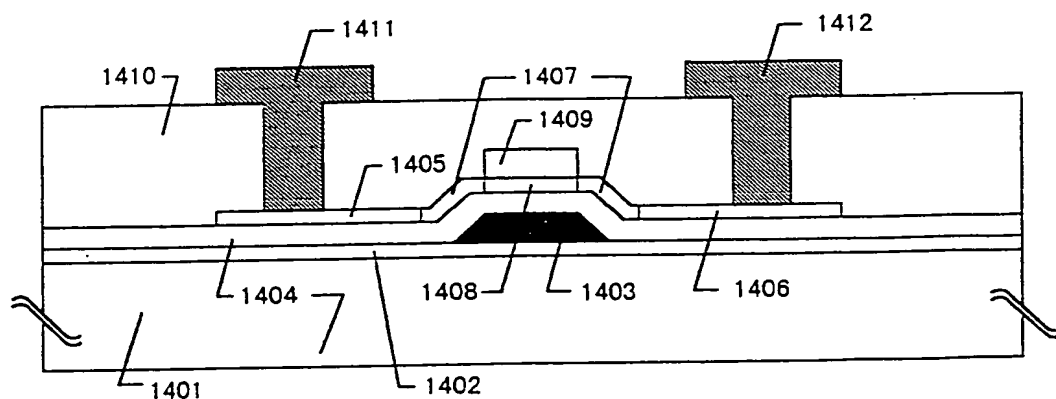
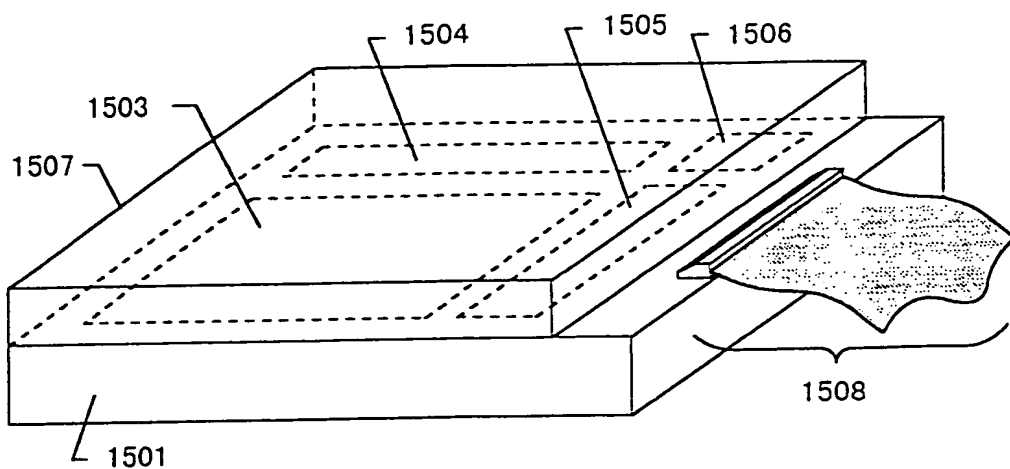


Fig. 14



- | | | | |
|------|----------------------|------|--|
| 1401 | SUBSTRATE | 1407 | LDW CONCENTRATION IMPURITY REGION (LDD REGION) |
| 1402 | SILICON OXIDE FILM | 1408 | CHANNEL FORMATION REGION |
| 1403 | GATE ELECTRODE | 1409 | CHANNEL PROTECTION FILM |
| 1404 | GATE INSULATION FILM | 1410 | LAYER INSULATION FILM |
| 1405 | SOURCE REGION | 1411 | SOURCE ELECTRODE |
| 1406 | DRAIN REGION | 1412 | DRAIN ELECTRODE |

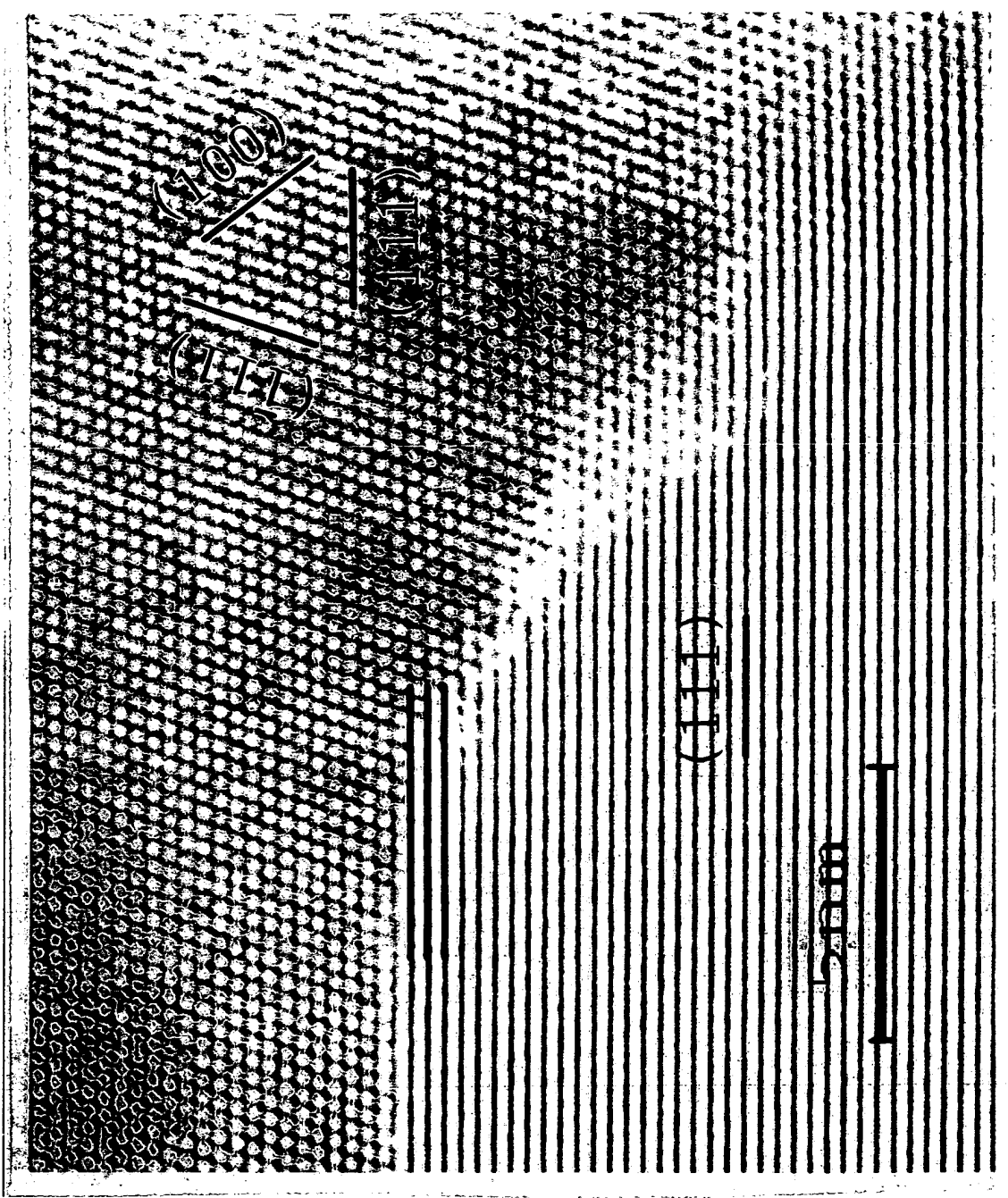
Fig. 15



1501 INSULATING SUBSTRATE	1505 SOURCE-SIDE DRIVING CIRCUIT
1503 PIXEL MATRIX CIRCUIT	1506 LOGIC CIRCUIT
1504 GATE-SIDE DRIVING CIRCUIT	1507 COUNTER SUBSTRATE
1508 FPC	

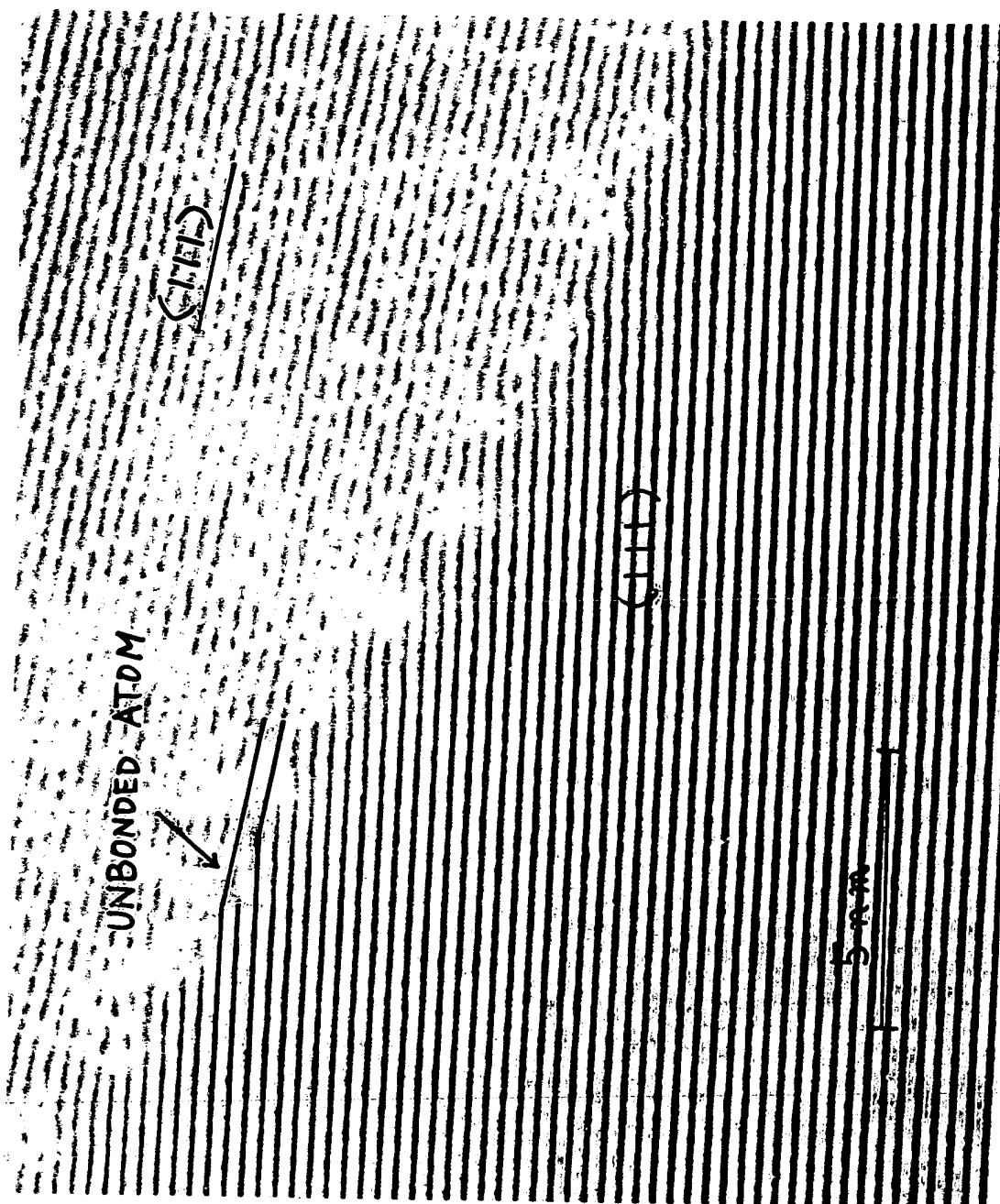
66220" 5095250

Fig. 16



66220" 50555260

Fig. 17



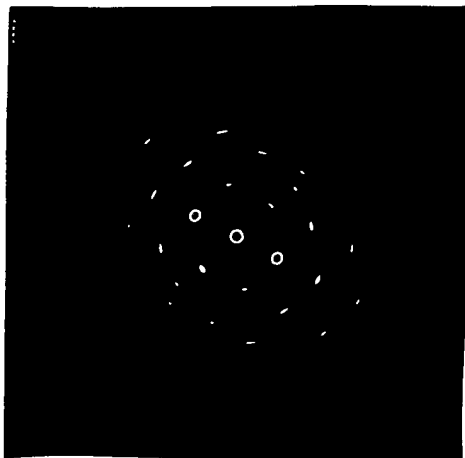


Fig. 18A



Fig. 18B

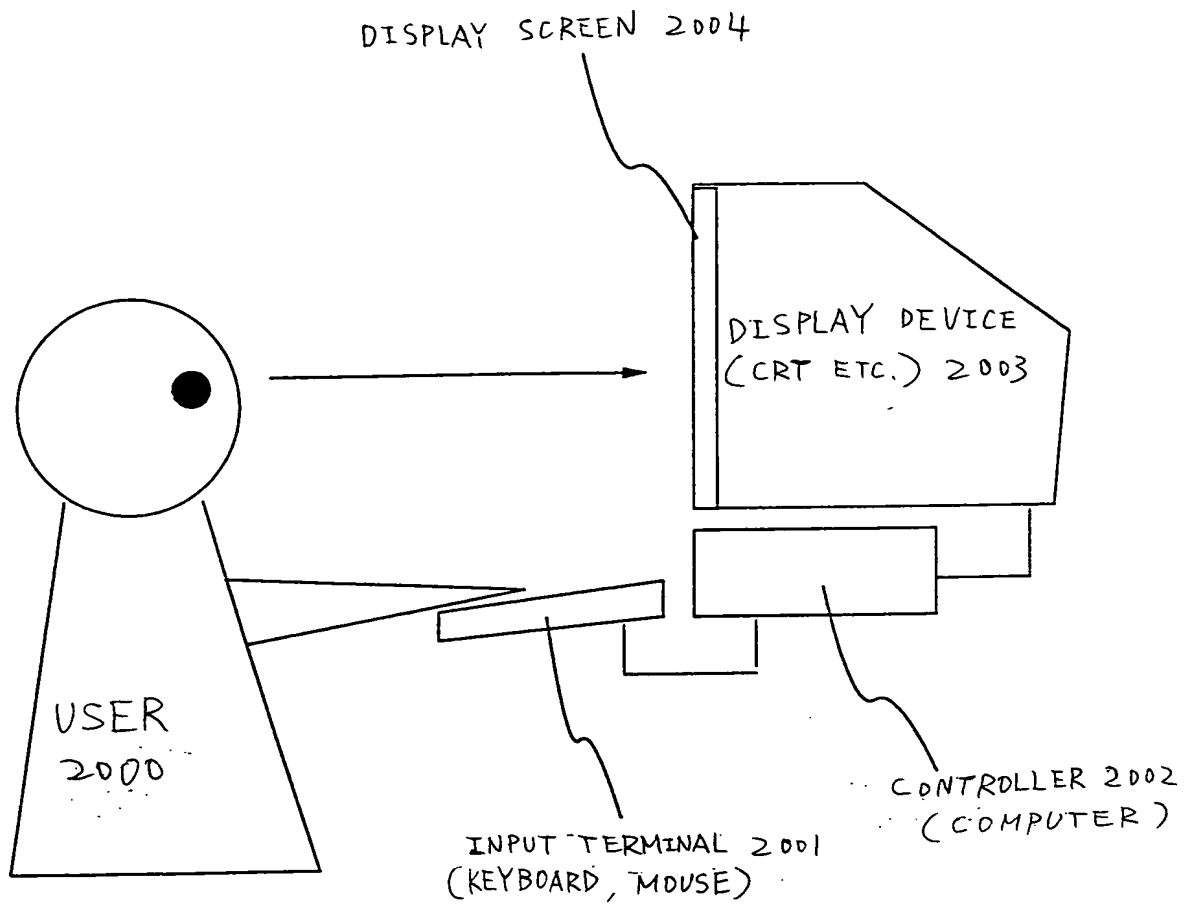
66666 909090

Fig. 19A



Fig. 19B

Fig. 20



SCHEMATIC VIEW OF PRIOR ART INFORMATION
PROCESSING APPARATUS.